Image AT/2814

Serial Nr.: 09/627,979
Art Unit: 2814

UPA-00156

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:	**09/627,979**	Examiner:	**DiLinh Nguyen**
Inventor:	**Randy H. Y. Lo, Chi-Chuan Wu and Ssu-Cheng Lai**		
Filed:	**July 28, 2000**	Art Unit:	**2814**
Title:	**Method Of Packaging Multi Chip Module**		

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Signature

Mar. 29, 2004
Date

BRIEF ON APPEAL

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the rejection of office action dated **12/18/2003** for the above identified application. A Credit Card Payment Form PTO-2038 for the payment of **$330** is enclosed for the required fee set forth in 37 CFR 1.17.

(1) Real Party in Interest

The real party in interest is **Randy H. Y. Lo, Chi-Chuan Wu and Ssu-Cheng Lai**.

(2) Related Appeals and Interferences

None.

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(3) Status of Claims

Claims 1-40, 46 and 55 were canceled. Claims 41-45, 47-54, and 56-57 are pending and rejected multiple times in the Office Actions. Claims 41-45, 47-54, and 56-57 are on appeal.

(4) Status of Amendments

No amendment has been filed subsequent to the rejection dated **12/18/2003**.

(5) Summary of Invention

The present invention is a multi-chip module package comprising at least one chip package 371, 372 and a multi-chip module substrate 31 enclosed by a package material 34 (page 2, lines 17-20; FIGs. 3A, 3C, 3D and 3E). Each chip package 371, 372 is a burn-in tested, function tested and already packaged chip module that has a bare chip 22 and a chip substrate 21 packaged and enclosed therein (page 5, line 15 to page 6, line 6; FIGs. 2A-2B). In one embodiment, the multi-chip module comprises a multi-chip module substrate 31, at least two chip packages 371, 372, a plurality of electrical connect points electrically connecting the chip packages 371, 372 with the multi-chip module substrate 31, a plurality of electrical connect pins 33, and a package material 34 enclosing the multip-chip module substrate 31, the electrical connect points and the chip packages 371, 372 (page 6, lines 14-20; FIG. 3A). In another embodiment, the multi-chip module comprises a bare die 321 and at least one chip package 372 (page 7, lines 8-13; FIG. 3C).

(6) Issues

Whether Claims 41, 47-49 and 56-57 are patentable under 35 U.S.C. 103(a) over

Akram et al. (US Patent No. 5,994,166) in view of Rostoker et al. (US Patent No. 5,648,661).

Whether Claims 42-44 and 51-53 are patentable under 35 U.S.C. 103(a) over Akram et al. (US Patent No. 5,994,166) in view of Rostoker et al. (US Patent No. 5,648,661) and further in view of Chen et al. (US Patent No. 6,214,642).

Whether Claims 45 and 54 are patentable under 35 U.S.C. 103(a) over Akram et al. (US Patent No. 5,994,166) in view of Rostoker et al. (US Patent No. 5,648,661) and further in view of Applicant Admitted Prior Art.

Whether Claims 49-50 and 56-57 are patentable under 35 U.S.C. 103(a) over Tanioka (US Patent No. 5,784,264) in view of Rostoker et al. (US Patent No. 5,648,661).

Whether Claims 51-53 are patentable under 35 U.S.C. 103(a) over Tanioka (US Patent No. 5,784,264) in view of Rostoker et al. (US Patent No. 5,648,661) and further in view of Chen et al. (US Patent No. 6,214,642).

Whether Claim 54 is patentable under 35 U.S.C. 103(a) over Tanioka (US Patent No. 5,784,264) in view of Rostoker et al. (US Patent No. 5,648,661) and further in view of Applicant Admitted Prior Art.

(7) Grouping of Claims

Claims 41-45 and 47-48 stand together in one group. Claims 49-54 and 56-57 stand together in the other group.

(8) Argument

The gist of this invention is to provide a multi-chip package structure that integrates at least an already packaged chip module onto the substrate of the multi-chip package structure. By integrating a packaged chip module, the yield of the multi-chip package is greatly increased because the packaged chip module has passed both burned-in and function test. Conventionally in the prior arts, only bare die or dice are used in a multi-chip package structure which often results in low yield in that the bare die or dice may be defective.

Applicants like to point out that **a bare die/chip is a semiconductor die cut from a wafer**. **A bare die/chip or a semiconductor die is different from a packaged chip module** in that a packaged chip module is a finished chip package that comprises a bare die embedded within the package, burn-in tested and function tested. **In other words, a packaged chip module is a protected module which has a good die embedded therein and guaranteed to be functional but a bare chip is neither tested nor protected and may be already defective.**

There are several advantages in using a packaged chip module rather than a bare chip in packaging a multi-chip module. **One is that it avoids the possibility of packaging a bare chip that may not be functional at all in the first place. The other is that the packaged chip module is much better protected than a bare chip from being damaged during the multi-chip packaging process.** Because a multi-chip module comprises multiple chips and is usually a high cost product, having high yield is very important in manufacturing. None of the prior arts including those cited by the Examiner has ever taught, suggested or anticipated the use of a packaged chip module in

packaging a multi-chip module. In the following, the teaching of the prior arts cited by the examiner will be more specifically excerpted and compared with the examiner's comments to elucidate the difference between the prior arts and the instant invention with respect to each ground of rejection.

- **Rejection of Claims 41, 47-49 and 56-57 under 35 U.S.C. 103(a) over Akram et al. in view of Rostoker et al.**

Akram et al. teach a semiconductor package comprising multiple stacked substrates having flip chips attached to the substrates with chip on board assembly technique to achieve dense packaging. The key subject matter in the art of Akram et al. is to stack multiple substrates of **bare chips** in the vertical direction to achieve high density.

On pages 2-3 of the office action, the Examiner rejects the base claims 41 and 49 by stating that "Akram et al. disclose a semiconductor device (cover fig.) comprising a multi-chip module substrate 102; at least a bare chip 162; at least two **chip pacakges, each of the chip packages being a packaged chip module** having a bare chip 150, 128 and a chip substrate packaged 140, 116 and enclosed therein 170; ...".

Applicants respectfully contend that the Examiner's statement is not the true disclosure of Akram et al. With reference to col. 6 in the disclosure of Akram et al., what is really disclosed is "a plurality of **first semiconductor dice 128 (col. 6, line 13), a plurality of second semiconductor dice 150 (col. 6, line 38), ..., or a plurality of fourth semiconductor dice 474 (col. 8, line 23), ...**". It is clear from either the cover figure or the detailed description, only **semiconductor dice** are used in the stacked

substrate chip assembly. Throughout the disclosure of Akram et al., there is no teaching of **"chip packages, each being a packaged chip module"** **as claimed in claims 41 and 49**.

Referring to col. 6, line 26 and lines 61-62 of Akram et al., "Furthermore, an encapsulation material 172 may cover the **stack dice portion** of the stacked assembly 100". Referring further to the abstract of Akram et al., it reads "A semiconductor package comprising multiple stacked substrate having **flip chips** attached to the substrate with **chip on board** assembly techniques to achieve dense package". It is common knowledge for a person with ordinary skill in the art of semiconductor to realize the difference between a chip (bare die) and a chip package. Applicants respectfully contend that the examiner's statement is unwarranted because all the disclosure of Akram et al. only refers to **semiconductor dice, chip or chip on board** which is certainly different from a **chip package**.

Rostoker et al. disclose a technique for individually electronically selecting unsingulated dies on a wafer for testing. The disclosed art does not teach or suggest any multi-chip module packaging. Applicants also like to point out that the art of Rostoker et al. is for **testing unsingulated dies** on a wafer that is completely different from the art of **testing a chip scale package** in the semiconductor industry. As recited in claim 41, "**said at least two chip packages having been burn-in tested and function tested"** is the subject matter of this invention that is very different from the teaching of Rostoker et al. There is absolutely no teaching or suggestion to enclose or package **a packaged chip module having a bare chip and a chip substrate packaged and enclosed therein**.

From the above discussion, it is evident that none of the cited prior arts discloses or suggests the limitation that the multi-chip package structure comprises **at least two chip packages, each of said chip packages being a packaged chip module having a bare chip and a chip substrate packaged and enclosed therein, said at least two chip packages having been burn-in tested and function tested** as claimed in claim 41. The independent claim 49 includes similar limitations. Both claims 41 and 49 should be patentable under 35 U.S.C. 103(a) over Akram et al. in view of Rostoker et al. By virtue of dependency, claims 47, 48, 56 and 57 should be patentable because Examiner's rejection presumes that their base claims 41 and 49 are not patentable.

- **Rejection of Claims 42-44 and 51-53 under 35 U.S.C. 103(a) over Akram et al. in view of Rostoker et al. and Chen et al.**

Examiner's rejection presmues that the independent claims 41 and 49 are not patentable. From the above discussion, both claims 41 and 49 should be patentable under 35 U.S.C. 103(a) over Akram et al. in view of Rostoker et al. By virtue of dependency, claims 42-44 and 51-53 should also be patentable.

- **Rejection of Claims 45 and 54 under 35 U.S.C. 103(a) over Akram et al. in view of Rostoker et al. and APAA**

Examiner's rejection presmues that the independent claims 41 and 49 are not patentable. From the above discussion, both claims 41 and 49 should be patentable under 35 U.S.C. 103(a) over Akram et al. in view of Rostoker et al. By virtue of dependency, claims 45 and 54 should also be patentable.

- **Rejection of Claims 49-50 and 56-57 under 35 U.S.C. 103(a) over Tanioka in view of Rostoker et al.**

On pages 4-5 of the office action, the Examiner rejects the claims 49-50 and 56-57 by stating that "Tonika discloses a multi-chip module package structure (fig. 1, column 1, lines 39 et seq.) comprising: a multichip module substrate 10 (column 1, line 41); at least a bare chip 7, at least one chip package being a packaged chip module having a bare chip 2 and a chip substrate packaged 11 and enclosed therein; ...".

Applicants respectfully contend that the Examiner has mis-interpreted the true disclosure of Tanioka which teaches a thin **multi-layer board** 11 formed on a thick multi-layer board 10 and a multi-layer hybrid circuit formed by the wire-bonding of "bare chips" and the mounting of chip parts (col. 1, lines 39-47). Tanioka **does not teach any chip package being a packaged chip module having a bare chip and a chip substrate packaged and enclosed therein, said at least one chip package having been burn-in tested and function tested**. The bare chip 2 and the multi-layer board 11 are encapsulated while they are mounted on the multi-layer board 10. It is not a chip package having been packaged and burn-in tested in the package before being put on the multi-chip substrate as claimed in the instant invention.

As discussed earlier, Rostoker et al. do not teach or suggest any multi-chip module packaging. The art of Rostoker et al. is for **testing unsingulated dies** on a wafer that is completely different from the art of **testing a chip scale package** which is done after the dies have been cut, separated and packaged in the semiconductor industry. As recited in claim 49, "**said at least one chip package having been burn-in tested and**

function tested" is the subject matter of this invention that is very different from the teaching of Rostoker et al.

From FIG. 1 of Tanioka's art, it can be seen that the bare chip 2 and thin multi-layer board 11 are encapsulated directly above the multi-layer board 10 and the encapsulation material also covers the multi-layer board 10. **There does not exist any chip package being a packaged chip module which has been burn-in tested and function tested.** Consequently, the combination of Rostoker et al. and Tanioka can not reach the subject matter of claim 49 that recites "**at least one chip packaging having been burn-in tested and function tested**".

From the above discussion, it is evident that none of the cited prior arts discloses or suggests **packaging a multi-chip substrate and a packaged chip package that has been burn-in tested and function tested** of claim 49. Applicants respectfully submit that claim 49 is patentable under U.S.C. §103(a) over Tanioka in view of Rostoker et al. By virtue of dependency, claims 50 and 56-57 should also be patentable.

- **Rejection of Claims 51-53 under 35 U.S.C. 103(a) over Tanioka in view of Rostoker et al. and Chen et al.**

Examiner's rejection presmues that the independent claim 49 is not patentable. From the above discussion, claim 49 should be patentable under 35 U.S.C. 103(a) over Tanioka in view of Rostoker et al. By virtue of dependency, claims 51-53 should also be patentable.

- **Rejection of Claim 54 under 35 U.S.C. 103(a) over Tanioka in view of Rostoker**

et al. and APAA

Examiner's rejection presmues that the independent claim 49 is not patentable. From the above discussion, claim 49 should be patentable under 35 U.S.C. 103(a) over Tanioka in view of Rostoker et al. By virtue of dependency, claim 54 should also be patentable.

(9) Appendix

The claims on appeal are as follows:

41. A multi-chip module package structure comprising:

a multi-chip module substrate;

at least two chip packages, each of said chip packages being a packaged chip module having a bare chip and a chip substrate packaged and enclosed therein, said at least two chip packages having been burn-in tested and function tested;

a plurality of electrical connect points electrically connecting said chip packages with said multi-chip module substrate;

a plurality of electrical connect pins; and

a package material enclosing said multi-chip module substrate, said connect points and said chip packages;

wherein said multi-chip module package structure is a ball grid array package.

42. The multi-chip module package structure as claimed in claim 41, wherein each of said chip packages is a chip-scale package or a wafer level chip-scale package.

43. The multi-chip module package structure as claimed in claim 41, wherein at least one of said chip packages is a chip-scale package with wire bonding.

44. The multi-chip module package structure as claimed in claim 41, wherein at least one of said chip packages is a chip-scale package with flip chip bonding.

45. The multi-chip module package structure as claimed in claim 41, wherein at least one of said chip packages is a chip-scale package with central pad bonding.

47. The multi-chip module package structure as claimed in claim 41, wherein said plurality of electrical connect pins are solder balls.

48. The multi-chip module package structure as claimed in claim 41, wherein said plurality of electrical connect points are solder balls or gold wires.

49. A multi-chip module package structure comprising:

a multi-chip module substrate;

at least a bare chip;

at least one chip package being a packaged chip module having a bare chip and a chip substrate packaged and enclosed therein, said at least one chip package having been burn-in tested and function tested;

a plurality of electrical connect points electrically connecting said bare chip and said at least one chip package with said multi-chip module substrate;

a plurality of electrical connect pins; and

a package material enclosing said multi-chip module substrate, said connect points, said bare chip and said at least one chip package;

wherein said multi-chip module package structure is a ball grid array package.

50. The multi-chip module package structure as claimed in claim 49, wherein said bare chip is bonded to said multi-chip module substrate by wire bonding or flip chip bonding.

51. The multi-chip module package structure as claimed in claim 49, wherein said at least one chip package is a chip-scale package or a wafer level chip-scale package.

52. The multi-chip module package structure as claimed in claim 49, wherein said at least one chip package is a chip-scale package with wire bonding.

53. The multi-chip module package structure as claimed in claim 49, wherein said at least one chip package is a chip-scale package with flip chip bonding.

54. The multi-chip module package structure as claimed in claim 49, wherein said at least one chip package is a chip-scale package with central pad bonding.

56. The multi-chip module package structure as claimed in claim 49, wherein said plurality of electrical connect pins are solder balls.

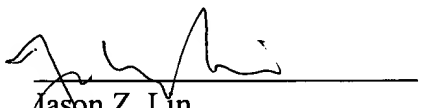
57. The multi-chip module package structure as claimed in claim 49, wherein said plurality of electrical connect points are solder balls or gold wires.

REMARKS

To summarize, appellants submit that claims claims 41-45, 47-54, and 56-57 are patentable because none of the cited prior arts teaches or suggests a multi-chip package structure comprising **at least one chip package being a packaged chip module having a bare chip and a chip substrate packaged and enclosed therein, and the chip package having been burn-in tested and function tested**.

If the Board agrees with the discussion above, claims 41-45, 47-54, and 56-57 should be allowed on appeal. Accordingly, the reversal of the Examiner by the honorable Board of Appeals is respectfully solicited.

Respectfully submitted,



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